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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,161	08/08/2001	Stephen Clark Purcell	69102 278147	3092

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EXAMINER	
FERRIS III, FRED O	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 02/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,161	PURCELL ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-14,27,28,32,34 and 37* is/are rejected.

7)☒ Claim(s) *10,11,15-26,29-31,33,35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-37 have been presented for examination based on applicant's amendment filed 16 November 2005. Claims 1-9, 12-14, 27, 28, 32, 34, and 37 remain rejected by the examiner. Claims 10, 11, 15-26, 29-31, 33, 35, and 36 are objected to.

Response to Arguments

2. Applicant's arguments filed 16 November 2005 have been fully considered.

Regarding applicant's response to 101 rejection: The examiner withdraws the 101 rejection in view of applicants amendment to the claims filed 16 November 2005.

Regarding applicants response to 103(a) rejection: The examiner maintains that the amendment to independent claims 1, 14,and 28 has not rendered the claimed subject matter non-obvious over the prior art. Applicants first argue that the figures of prior art (Giacalone) do not disclose the storage of intermediate data in a left and right memory bank, and therefore do not disclose or suggest Wallace tree stages, or final adder configuring logic circuits to store the intermediate data in a manner to simulate a layered tree structure. The examiner first notes that applicants appear to be engaging in piecemeal analysis by arguing that Giacalone does not teach the claimed limitations relating to configuring logic circuits to store the intermediate data. In this case, the examiner has relied upon Giacalone for disclosing teachings such as the use of Wallace tree stages (Fig. 24) and summing (adder) circuits (Figs. 14, 15, 21) as noted below under 103(a) rejections. Han (not Giacalone) teaches elements relating to configuring logic circuits to store intermediate data (para:0060) as also noted below. One cannot

show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicants further argue that the figures disclosing the accumulator of Giacalone do not disclose the use of a left and right memory bank. The examiner first submits that the claimed term "memory bank" can be interpreted to include nearly any configuration of logic elements capable of storing a result. (i.e. a group of electrical devices connected to form a memory, See: "bank" (1), Microsoft Computer Dictionary, 1997). In this case Giacalone teaches groups of registers (memory elements) arranged to form a bank of memory elements (Fig. 24). Giacalone therefore renders obvious the claimed elements relating to a memory bank storing layers simulating a layered tree structure (See: Figs. 20, 24) Second, applicants have merely claimed a duplicate left and right memory bank both storing the intermediate results.

MPEP 2144.04 recites the following:

> *"B. Duplication of Parts*
> *In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) (Claims at issue were directed to a water-tight masonry structure wherein a water seal of flexible material fills the joints which form between adjacent pours of concrete. The claimed water seal has a "web" which lies ** in the joint, and a plurality of "ribs" ** >projecting outwardly from each side of the web into one of the adjacent concrete slabs. <The prior art disclosed a flexible water stop for preventing passage of water between masses of concrete in the shape of a plus sign (+). Although the reference did not disclose a plurality of ribs,* ***the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.)****."*

Here the memory banks appear to be a mere duplication of parts since there is no claimed operational significance between the two.

The remaining thrust of applicants arguments center around arguing that the prior art does not teach the claimed elements of "selecting a left (or right) side source for among a zero value, the initial input values, or a set of intermediate result values". Regarding selecting (left/right source) from among a zero value, the initial input values, or a set of intermediate values, the examiner submits that the selection of a "zero value" is necessary in order to clear (i.e. flush) the memory bank(s) (See: "flush (2), Microsoft Computer Dictionary 1997) and would have therefore been knowingly incorporated by a skilled artisan. Selecting initial and intermediate values are disclosed by the prior art as noted below. The examiner also notes that claims 14 and 28 merely recite left and right input selectors for directing between intermediate results and initial values. However, there are no limitations recited in the language of the claims that specifically require that the intermediate results come from a left or right "memory bank". These limitations therefore remain obvious in view of Giacalone's teaching of controlling a first and second (i.e. a first and second source, equivalent to left and right) accumulator memory bank (CL28-L59-67, Figs. 20-24) and directing (redirecting and selecting) the result into various fields. (CL23-L31-47, Fig. 17C) The recitation of "streaming initial input values (original order) into an input of the accumulator" is interpreted by the examiner as simply providing (i.e. inputting) the initial input values to the accumulator and would therefor be an operationally necessary part of the accumulator disclosed by Giacalone (Fig. 24) or

Han (Fig. 11). MPEP 2106 recites the following supporting rationale for this interpretation:

> "While it is appropriate to use the specification to determine what applicant intends a term to mean, a positive limitation from the specification cannot be read into a claim that does not impose that limitation. A broad interpretation of a claim by Office personnel will reduce the possibility that the claim, when issued, will be interpreted more broadly than is justified or intended. An applicant can always amend a claim during prosecution to better reflect the intended scope of the claim."

For the reasons set forth above, and below under 103(a) rejections, the examiner maintains the rejection of claims 1-9, 12-14, 27, 28, 32, 34, and 37 as obvious in view of Giacalone and Han. However, in view of applicant's arguments relating to Figures 1, 2, 5A, 17C, 20, 21, 22, the amendment to the claims, and further review of the prior art, the examiner withdraws the rejection of claims 10, 11, 15-26, 29-31, 33, 35, and 36 which now stand objected to as dependent from a rejected base claim. (See: Allowable Subject Matter below)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-9, 12-14, 27, 28, 32, 34, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent issued to Giacalone et al in view of U.S. Patent Application Publication 2002/0039386 A1 issued to Han et al.

Regarding independent claim 1: Giacalone teaches constructing an accumulator inclusive of a layered tree structure (CL5-L55-67, CL6-L43-67, Figs. 1, 2) controlling flow of the accumulation data and a programmed (i.e. directed) structure (CL5-L39-67, CL15-L17-55, CL23-L3-53, Figs. 1, 7A, 17A-C) for controlling the string length inputs (CL7-L61 to CL8-L5, Fig. 2) and maintaining control of the layers within the tree structure. (CL11-L29 to CL12-L7, Figs. 4A-C).

Giacalone does not explicitly disclose a layered tree structure configured to contain the intermediate accumulation result.

Han also teaches constructing an accumulator inclusive of a layered tree structure, but further teaches a tree structure that is configured to buffer (contain) the intermediate accumulation results (Para: 0060, 0053, Fig. 11).

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Giacalone relating to constructing an accumulator inclusive of a layered tree structure controlling and buffering the accumulation data, with the teachings of Han relating to a tree structure that is configured to buffer (contain) the intermediate accumulation results, to realize the

elements of the claimed invention. An obvious motivation exists since, in this case, the Giacalone reference teaches to the Han reference, and the Han reference teaches to the Giacalone reference. Specifically, both Giacalone and Han teach and accumulator design including a controlling tree structure and both are used in the same technological arena as noted above. Giacalone teaches to Han because Giacalone teaches a layered tree structure for controlling and buffering the accumulation data as does Han (See: Giacalone, Summary of Invention). Han teaches to Giacalone because Han specifically teaches a tree structure that is configured to buffer (contain) the intermediate accumulation results. (See: Han: 0060, Fig. 11) Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Giacalone/Han, Background/Abstract) Accordingly, a skilled artisan tasked with realizing an accumulator inclusive of a layered tree structure configured to buffer the intermediate accumulation results, and having access to the teachings of Giacalone and Han, would have knowingly modified the teachings of Giacalone with the teachings of Han (or visa versa) to realize the claimed elements of the present invention while reducing the cost and development time.

Regarding dependent claims 2-4: Giacalone teaches using a first and second (i.e. equivalent to left and right) accumulator memory bank (CL28-L59-67, Figs. 20-24) processed in first in, first out (i.e. FIFO) order (CL3-L35-41).

Regarding dependent claims 5-9, and 12: Giacalone teaches controlling a first and second (i.e. a first and second source, equivalent to left and right) accumulator memory bank (CL28-L59-67, Figs. 20-24) and directing (redirecting and selecting) the

result into various fields. (CL23-L31-47, Fig. 17C) Selecting "zero" would obviously be necessary in order to flush (clear) the memory bank. Han discloses single adder control (Fig. 6) and would have knowingly been incorporated by a skilled artisan using the reasoning cited above.

Regarding dependent claims 13, 27, and 37: These dependent claims recite a floating-point input value and would have knowingly been incorporated by a skilled artisan in order to accommodate the well-known numerical format (i.e. a mantissa and exponent format) for representing very large and very small real numbers. (See: "floating point", Microsoft Computer Dictionary, 1997)

Regarding independent claims 14 and 28: As cited above, Giacalone renders obvious the limitations relating to constructing an accumulator inclusive of a layered tree structure (CL5-L55-67, CL6-L43-67, Figs. 1, 2) controlling flow of the accumulation data and a programmed (i.e. directed) structure (CL5-L39-67, CL15-L17-55, CL23-L3-53, Figs. 1, 7A, 17A-C) for controlling the string length inputs (CL7-L61 to CL8-L5, Fig. 2) and maintaining control of the layers within the tree structure. (CL11-L29 to CL12-L7, Figs. 4A-C) In addition, Giacalone teaches an accumulator method capable of accommodating larger arbitrary input values (i.e. N-length strings) (CL8-L3-5, Fig. 2) as recited as an additional element in independent claim 14.

Giacalone does not explicitly disclose a layered tree structure configured to contain the intermediate accumulation result.

Han also teaches constructing an accumulator inclusive of a layered tree structure, but further teaches a tree structure that is configured to buffer (contain) the intermediate accumulation results (Para: 0060, 0053, Fig. 11).

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Giacalone relating to constructing an accumulator inclusive of a layered tree structure controlling and buffering the accumulation data, with the teachings of Han relating to a tree structure that is configured to buffer (contain) the intermediate accumulation results, to realize the elements of the claimed invention. An obvious motivation exists since, in this case, the Giacalone reference teaches to the Han reference, and the Han reference teaches to the Giacalone reference. Specifically, both Giacalone and Han teach an accumulator design including a controlling tree structure and both are used in the same technological arena as noted above. Giacalone teaches to Han because Giacalone teaches a layered tree structure for controlling and buffering the accumulation data as does Han (See: Giacalone, Summary of Invention). Han teaches to Giacalone because Han specifically teaches a tree structure that is configured to buffer (contain) the intermediate accumulation results. (See: Han: 0060, Fig. 11) Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Giacalone/Han, Background/Abstract) Accordingly, a skilled artisan tasked with realizing an accumulator inclusive of a layered tree structure configured to buffer the intermediate accumulation results, and having access to the teachings of Giacalone and Han, would have knowingly modified the teachings of

Giacalone with the teachings of Han (or visa versa) to realize the claimed elements of the present invention while reducing the cost and development time.

Regarding claims 32 and 34: Giacalone teaches elements relating to controlling accumulator input delay (CL16-L8-55, Fig. 8, 7A), phase count (Figs. 2, 5, 8, i.e. odd/even input), and accumulating queue (CL23-L53-67, CL25-L57-67, Figs 17C, 22).

Allowable Subject Matter

4. Claims 10, 11, 15-26, 29-31, 33, 35, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In this case the prior art of record does not explicitly disclose the additional arrangement of elements relating to data flow control fields including cycle type, routing field, and layer field (clams 10-11), passing based on phase counting (without delay) or even phase count available to be accumulated with odd phase count (claims 15-26, 33), or memory bank ports coupled to adder with control device output port coupled to selection mechanism (claims 29-31, 35, 36).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP*

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Accelerating Pipelined Integer and Floating-Point Accumulations in Configurable Hardware with Delayed Addition Techniques", Luo et al, IEEE Transactions on Computers, Vol. 49, No. 3, March 2000 teaches floating point tree based accumulators.

"Architectures for Pipelined Wallace Tree Multiplier-Accumulators", Pang, IEEE CH2909-0/90/0000/0247, IEEE 1990 teaches floating point tree based accumulators.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry

of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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